Amendments to the Specification:

Please replace paragraph [0012] with the following amended paragraph:

[0012] According to the claimed invention, a chip-packaging with bonding options having a plurality of package substrates comprises a first package substrate, a second package substrate, a chip comprising a plurality of the bonding pads and mounted on first package substrate wherein one bonding pad is connected to the first package substrate and another bonding pad is connected to the second package substrate, and a lead ~~frame~~ connected to one bonding pad.

Please add the following two new paragraphs [0019.1] and [0019.2] after paragraph [0019]:

[0019.1] Fig.7 is a cross-sectional view of the option architecture 50 of Fig.4.

[0019.2] Fig.8 is a cross-sectional view of the option architecture 100 of Fig.6.

Please replace paragraph [0021] with the following amended paragraph:

[0021] Please refer to Fig.4. Fig.4 illustrates the bonding option architecture 50 of the present invention providing three connection points for the bonding pads. The bonding option architecture 50 comprises a plurality of ~~lead frames~~ leads 52, a plurality of bonding wires 54, a chip 56, a first package substrate 58, and a second package substrate 60. The chip 56 comprises a plurality of bonding pads 62. The bonding pads 62 are set inside the chip 56 and surround the chip 56, providing the outlets of input/output ends of the chip 56. The ~~lead frames~~ leads 52 distributed around and outside the chip 56 are connected to the bonding pads 62 inside the chip 56 through bonding wires 54. The bonding pads 62 are like the connection points which connect the inside circuit of the

chip 56 to the outside system while the ~~lead frames~~ leads 52 are like the connection points which connect the outside system to inside circuit of the chip 56. The bonding option architecture 50 lets the input/output signals of the chip to communicate with outside circuitry and provides chip testing.

Please replace paragraph [0022] with the following amended paragraph:

[0022] The first package substrate 58 and the second package substrate 60 are the bottom plates of the chip package. The shape of the package substrate is shown in Fig.4. The chip 56 is mounted above the second package substrate 60, which the first package substrate 58 immediately surrounds. The outside periphery is the second package substrate which also surrounds the first package substrate. In this arrangement of package substrates, one can see at least one portion of the first package substrate 58 and at least one portion of the second package substrate 60 when looking outside from the chip in any direction. In other words, any bonding pad 62 approximates at least a portion of the first package substrate 58 and at least a portion of the second package substrate 60. Because a plurality of the ~~lead frames~~ leads 52 are distributed around the chip, the bonding pad 62 also approximates at least one lead ~~frame~~. Two package substrates are used here for providing two different voltages to the bonding option, wherein one package substrate has a high voltage and the other has a low voltage. For example, the first package substrate 58 is applied to the power supply and the second package substrate 60 is applied to the ground voltage.

Please add the following new paragraph [0022.1] after paragraph [0022]:

[0022.1] Please refer to Fig.7. Fig.7 is a cross-sectional view of the option architecture 50 of Fig.4. The chip 56 is shown mounted on the second package substrate 60, and the first package substrate 58 is formed in between sections of the second package substrate 60.

The chip 56 contains the plurality of bonding pads 62 around the perimeter of the chip 56, and the leads 52 are formed around the perimeter of the second package substrate 60.

Please replace paragraph [0023] with the following amended paragraph:

[0023] Please refer to Fig.5. Fig.5 illustrates the bonding option architecture of the present invention. The bonding option architecture in Fig.5 is the detailed illustration of Fig.4. Each marked item in Fig.5 of the same names with those in Fig.4 has the same functions. Besides, Fig.5 further shows a bonding option unit 80. The bonding option unit 80 is connected to the inside circuitry of the chip 56, and the bonding pad 62 is included in the bonding option unit 80. As mentioned before, the bonding option unit 80 is possibly connected to Enable, Disable, or to the other systems. Therefore, there are three connection points: the lead ~~frame~~ 52 for the first bonding option, the first package substrate 60 for the second bonding option, and the second package substrate 58 for the third bonding option near the bonding pad 62. The first bonding option provides outlets for input/output signals of the chip 56. The second bonding option and the third bonding option provide the voltage of the power supply and the voltage of the ground. In the preferred embodiment of the present invention, the first package substrate 58 serving as the second bonding option provides the power supply while the second package substrate 60 serving as the third bonding option provides the ground. Of course, the voltages that two package substrates have can be exchanged. In this embodiment, when the bonding option unit 80 needs a voltage of the power supply, the bonding wire 54 connects the bonding pad 62 to the first package substrate 58 so that the voltage of the power supply is applied to the bonding option unit 80 and reaches the inside circuitry. In another case, when the bonding option unit 80 has to be connected to the ground, the bonding wire 54 connects the bonding pad 62 to the second package substrate 60 so that the bonding option unit 80 has the ground voltage. In the last case, the bonding option unit 80 is connected to the lead ~~frame~~ 52 through the bonding wire 54 for generating a transmission

trace between the inside chip and the outside systems. Thus, the present invention utilizes only one lead ~~frame~~ to provide three functions of a bonding option, which not only removes the disadvantages of difficult arrangement of many ~~lead frames~~ leads in the prior art, but also lowers the production cost by reducing the number of ~~lead frames~~ leads.

Please replace paragraph [0024] with the following amended paragraph:

[0024] Notice that the embodiment in Fig.5 sets up a single lead ~~frame~~ 52 for each bonding option unit 80. In fact, the present invention can be implemented using only one lead ~~frame~~ for a bonding option. However, the number of ~~lead frames~~ leads for a single bonding option unit 80 is not limited to one. Designers are free to set up any amounts of ~~lead frames~~ leads for one bonding option unit for some special purpose. Moreover, the preferred embodiment of the present invention utilizes two package substrates. In reality, a plurality of package substrates can be provided for the bonding option. Change of the number of the ~~lead frames~~ leads for each bonding unit or the number of the package substrates is included in the claimed range of the present invention if they reach the similar effects of the present invention.

Please replace paragraph [0025] with the following amended paragraph:

[0025] Please refer to Fig.6. Fig.6 illustrates another bonding option architecture 100. In this embodiment, the shape of the package substrate is modified. The bonding option architecture 100 comprises a first package substrate 90, a second package substrate 92, a chip 94, a plurality of the bonding pads 96, and a plurality of ~~lead frames~~ leads 98. The shape of the first package substrate 90 is different from that in Fig.4. The chip 94 is mounted on the first package substrate 90. The area of the first package substrate 90 is larger than that of the chip 94, and the first package substrate 90 extends outside the chip 94 so that the first package substrate 90 has enough area for a bonding wire to connect to.

The second package substrate 92 surrounds the first package substrate 90, and a plurality of the ~~lead frames~~ leads 98 are set on the periphery of the package substrate. In the bonding option architecture in Fig.6, each bonding pad 96 distributed around the chip 94 approximates three portions, which are the first package substrate 90, the second package substrate 92, and a lead ~~frame~~ 98. The three portions can be used as three connection points: the first bonding option, the second bonding option, and the third bonding option, for the bonding pad 96. The first package substrate and the second package substrate are connected to two different voltages, the power supply and the ground. The lead ~~frame~~ 98 serves as input/output outlets. Therefore, this embodiment implements functions of the bonding options. Of course, the package substrate has other changes in shapes, which is also included in the present invention.

Please add the following new paragraph [0025.1] after paragraph [0025]:

[0025.1] Please refer to Fig.8. Fig.8 is a cross-sectional view of the option architecture 100 of Fig.6. The chip 94 is shown mounted on the first package substrate 90, and the second package substrate 92 surrounds the first package substrate 90. The chip 94 contains the plurality of bonding pads 96 around the perimeter of the chip 94, and the leads 98 are formed around the perimeter of the second package substrate 92.

Please replace paragraph [0027] with the following amended paragraph:

[0027] Compared to the prior art, the present invention utilizes a plurality of package substrates as the voltage supply or the ground to implement bonding option without increasing additional ~~lead frames~~ leads. Therefore, the present invention has the following advantages: 1. Provide convenient testing and other functions for a chip, and let a single chip operate in different modes. 2. Make it easier to arrange ~~lead frames~~ leads because only one lead ~~frame~~ is needed for providing the voltage of the power supply and the

ground. 3. It is easier to use and maintain the bonding option. 4. Less number of ~~lead frames~~ leads to smaller layout area and lower production cost. The present invention reserves the advantages of the prior art and has additional advantages that the prior art cannot achieve.

Please replace the abstract of the disclosure with the following amended paragraph:

Chip-packaging with bonding options having a plurality of package substrates. The chip-packaging includes first and second package substrates, a chip, and a lead ~~frame~~. The chip having a plurality of bonding pads is mounted on the first package substrate. One of these bonding pads is connected to the first package substrate. Another bonding pad is connected to the second package substrate. The lead ~~frame~~ is connected to one bonding pad. The first and second package substrates have first and second voltages, respectfully. The first voltage and the second voltage are different, and each can be a GND voltage or a POWER voltage. With connection of these bonding pads with the lead ~~frame~~ or connection of these bonding pads with two package substrates, input ends or output ends in the chip could be connected to a GND voltage or a POWER voltage, or to one pin of the chip-packaging.